REMARKS

Claims 2, 3, 19 and 23-28 are pending. Claims 2, 3 and 28 are amended and claim 5 is hereby canceled.

Claim 3 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. The Examiner states that it appears that there is no support for the new limitation of "in the third step of etching the first insulation film, the first insulation film is etched to form the opening exposing in a part of a bottom thereof a second region of the semiconductor substrate, which is other than the first region, and exposing in another part of the bottom thereof the fourth insulation film."

Claim 3 was also rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that it is not clear how in the third step of etching the first insulation film, the first insulation film is etched to form the opening, exposing in a part of a bottom thereof a second region of the semiconductor substrate, which is other than the first region, and exposing in another part of the bottom thereof the fourth insulation film, and it is not clear if the fourth insulation film is formed only on the conductive pattern or over the whole substrate.

The limitation of "in the step of forming the fourth insulation film, the fourth insulation film is selectively formed over a side wall of the conductor pattern; and in the third step of etching the first insulation film, the first insulation film is etched to form the opening exposing in a part of a bottom thereof a second region of the semiconductor substrate, which is other than the first region,

and exposing in another part of the bottom thereof the fourth insulation film" of amended claim 3 can be read on, e.g., FIGs. 20B-21A. The insulation film 30 is selectively formed on a side wall of the gate electrode 20 (see, e.g., FIG. 3C). The insulation films 18 and 30 form the insulation film 42 (see, e.g., FIGs. 3C-4A). The opening 38 exposes the semiconductor substrate 10 and the insulation film 42 which is other than the region where the gate electrode 20 is formed. Accordingly, it is respectfrully submitted that claim 3 is in full compliance with 35 U.S.C. §112.

Claim 28 was rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states that it is not clear what "an etching rate of the second insulation film at the first step of etching the third insulation film" is, since the second and the third insulation films are etched with two separate etching steps according to claim 2.

According to the above-described amendments, "an etching rate of the second insulation film at the first step of etching the third insulation film" is changed to --an etching rate of the second insulation film when the second insulation film is etched with an etching condition at the first step of etching the third insulation film--. Favorable reconsideration is respectfuly requested.

Claims 2, 3, 5, 19 and 23-27 are rejected under 35 U.S.C. §102(e) as being anticipated by *Dennison et al.* (U.S. Patent No. 5,338,700). Favorable reconsideration of this rejection is requested in view of the amendments made herein.

As described above, Applicant has amended claim 2 to more distinctly claim the subject matter of the invention. Specifically, the applicant has further defined that the method further includes the steps of: "forming a conductive material in the hole to form a conductive plug of the

conductive material; forming over the third insulation film an interconnection pattern connected to the conductive plug; and forming a fifth insulation film over the interconnection pattern." As will be explained below, these features of claim 2 are distinct over *Dennison et al.*

The Examiner identified that the layer 52 in FIG. 4 of *Dennison et al.* corresponds to the third insulation film of the claimed invention. However, in *Dennison et al.*, the layer 52 is removed after the isolated cell capacitor storage electrode 62 has been formed (see, e.g., FIG. 5). Thus, in *Dennison et al.*, an interconnection pattern cannot be formed over the layer 52 after the formation of the isolated cell capacitor storage electrode 62. Additionally, the isolated cell capacitor storage electrode 62 would never be connected to the upper level interconnection, because the isolated cell capacitor storage electrode 62 is covered with the capacitor cell dielectric layer 68 and the conductive capacitor cell layer 70. *Dennison et al.* neither teaches nor suggests the interconnection pattern connected to the conductive plug and formed over the third insulation film, and the fifth insulation film formed over the interconnection pattern. Hence, the noted features, namely "forming a conductive material in the hole to form a conductive plug of the conductive material; forming over the third insulation film an interconnection pattern connected to the conductive plug; and forming a fifth insulation film over the interconnection pattern" are distinct over *Dennison et al.*

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. In view of the distinction of claim 2 noted above, at least one claim element is not present in Dennison et al. Hence, Dennison does not anticipate claim 2.

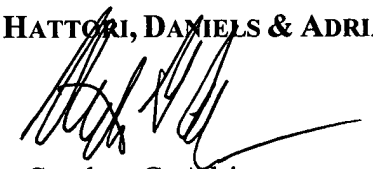
In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP



Stephen G. Adrian
Attorney for Applicants
Registration No. 32,878
Telephone: (202) 822-1100
Facsimile: (202) 822-1111

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